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09/994,233	11/26/2001	Michael A. Nix	X-1012 US	8295

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/994,233	NIX, MICHAEL A.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *1-12,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/17/03 has been entered.

Claim Objections

2. Claims 10 is objected to because of the following informalities: "having" on line 11 should be changed to --receiving-- because it is better to say that a control terminal of a transistor receiving a clock signal. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 16, "a clock terminal" is unclear antecedent basis because it is not clear whether it is the same as the clock terminal recited earlier in the claim (last line of independent claim 10). Also, "the control terminal" is also unclear antecedent basis because it is not clear which control terminal that the phrase refers to, i.e., the control terminal recites on line 11 of independent claim 10 or the control terminal recites on line 10 of claim 15.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara (USP 6,018,260).

With respect to claim 1, Figure 2 of the Gabara reference discloses a flip-flop circuit which includes: a differential output stage (140, 145, 110, 132) having differential first and second input terminals (IN and /IN) and complementary first and second output terminals (/OUT and OUT); a transistor (150, lines 38-43 of Col. 5) having a first current-handling terminal (115) connected to the first output terminal (OUT/), a second current-handling terminal (135) connected to the second output terminal (OUT), and a control terminal (terminal receiving the signal /CLK); and a cross-coupled circuit (105, 125) having a cross coupled transistor (105) configured to continuously receive power from a positive power supply voltage (VDD), wherein a gate of the cross-coupled transistor (105) is connected to the second output terminal (OUT).

With respect to claim 2, Figure 2 shows a clock terminal (/CLK) connected to the control terminal (control terminal of transistor 150).

7. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Choe (USP 6,373,292).

With respect to claim 1, Figure 5 of the Choe reference discloses a flip-flop circuit which includes: a differential output stage (right stage 40 that provides OUT and /OUT) having differential first and second input terminals (the gates of the n-channel transistors in the right stage 40 which are respectively connected to receive the outputs of the left stage 40) and complementary first and second output terminals (/OUT and OUT); a transistor (transistor 56 in the right stage 40, see Figure 2 for stage 40) having a first current-handling terminal connected to the first output terminal (/OUT), a second current-handling terminal connected to the second output terminal (OUT), and a control terminal (gate terminal receiving the signal /CLK); and a cross-coupled circuit (the two p-channel transistors in the right stage 40, see Figure 2 for stage 40, that are cross-coupled to the outputs /OUT and OUT) having a cross coupled transistor (the p-channel transistor in the right stage 40, see Figure 2 for stage 40, that has its gate directly connected to output OUT) configured to continuously receive power from a positive power supply voltage (VDD, see Figure 2 for stage 40), wherein a gate of the cross-coupled transistor is connected to the second output terminal (OUT).

With respect to claim 2, Figure 5 shows a clock terminal (/CLK) connected to the control terminal.

With respect to claim 3, Figure 5 shows a second transistor (n-channel transistor 56 of the left stage 40) having a third current-handling terminal connected to the first input terminal (one terminal of transistor 56 in the left stage 40 connected directly to a gate terminal of an n-channel transistor in the right stage 40), a fourth current-handling terminal connected to the second input

terminal (the other terminal of transistor 56 in the left stage 40 connected directly to another gate terminal of another n-channel transistor in the right stage 40), and a second control terminal (gate of 56 in the left stage 40).

With respect to claim 4, Figure 5 of the Choe reference includes a first clock terminal (/CLK) connected to the first-mentioned control terminal (gate of transistor 56 in the right stage 40 connected to receive clock signal /CLK) and a second clock terminal (/CLK) connected to the second control terminal (gate of n-channel transistor 56 in the left stage 40 connected to receive clock /CLK).

With respect to claim 6, Figure 5 of the Choe reference shows that the flip-flop circuit includes a differential input stage (left stage 40) having differential third and fourth input terminals (INPUT and /INPUT) and complementary third and fourth output terminals (the two outputs of left stage 40 which are directly connected to the inputs of right stage 40) connected to the first and second input terminals (the inputs of right stage 40), respectively.

With respect to claims 7-8, these claims are rejected for the same reasons as in claims 2-3, respectively.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-9 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Furuki (USP 5,384,493) in view of Choe (USP 6,373,292).

With respect to claim 1, Figure 6 of the Furuki reference discloses a flip-flop circuit includes a first stage (10b) and a second stage (10c), wherein the second stage (10c) includes a differential output stage (Q13-Q14) having differential first and second input terminals (OUT1, OUT2) and complementary first and second output terminals (OUT3, OUT4); and a cross coupled circuit (Q27, Q28) having a cross coupled transistor (Q27) configured to continuously receive power from a positive power supply voltage, wherein a gate of the control coupled transistor (Q27) is connected to the second output terminal (OUT4). Figure 6 of the Furuki reference does not disclose a transistor having a first current-handling terminal connected to the first output terminal (OUT3), a second current-handling terminal connected to the second output terminal (OUT4), and a control terminal (gate terminal receiving the signal /CLK). However, Figure 2 of the Choe reference discloses a differential circuit which includes a transistor (56) having a control terminal (gate), a first current-handling terminal connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of reducing power consumption and improving the speed of the circuitry (line 25 of Col. 2 to line 10 of Col. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the stages (10b and 10c) in the flip-flop circuit (Figure 6) of the Furuki reference with a transistor connected between the outputs of each differential stage (i.e., a transistor connected between nodes OUT1 and OUT2 in the differential stage 10b and its gate receives clock signal CLK because the transistor Q3 of the stage 10b receiving clock signal CLKb, and also another transistor connected between the output nodes OUT3 and OUT4 in the differential stage 10c and its gate receives clock signal /CLK because the transistor Q4 of the stage 10c receives clock signal CLK), as taught by the Choe

reference (transistor 56 in Figure 2 of Choe), for the purpose of reducing power consumption and improving the speed of the circuitry. Thus this modification/combination meets all the limitations of claim 1 because the stage 10c now also includes a transistor having a first current-handling terminal connected to the first output terminal (OUT3), a second current-handling terminal connected to the second output terminal (OUT4), and a control terminal (gate terminal receiving the signal /CLK).

With respect to claim 2, the modification/combination as discussed in claim 1 includes a clock terminal (/CLK) connected to the control terminal (clock terminal /CLK connected to the gate of the transistor connected between the output terminal OUT3 and OUT4).

With respect to claim 3, the above modification/combination shows a second transistor (the transistor connected between terminals OUT1 and OUT2 which having its gate receives clock CLK as discussed above) having a third current-handling terminal connected to the first input terminal (OUT1), a fourth current-handling terminal connected to the second input terminal (OUT2), and a second control terminal (the gate of the transistor connected to receive clock CLK).

With respect to claim 4, the above modification/combination includes a first clock terminal (/CLK) connected to the first-mentioned control terminal (gate of transistor connected between output terminals OUT3 and OUT4 of the stage 10c) and a second clock terminal (CLK) connected to the second control terminal (gate of the transistor connected between the outputs OUT1 and OUT2 of the stage 10b).

With respect to claim 5, the above modification/combination as discussed above meets the limitation that the first and second clock terminals are adapted to receive complementary clock signals.

With respect to claim 6, the above modification/combination as discussed above includes a differential input stage (10b) having differential third and fourth input terminals (D and Db) and complementary third and fourth output terminals (OUT1 and OUT2) connected to the first and second input terminals (OUT1 and OUT2 are the inputs of the stage 10c), respectively.

With respect to claims 7-9, these claims are rejected for the same reasons as in claims 2-5.

10. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (USP 5,777,491) in view of Choe (USP 6,373,292).

With respect to claim 10, Figure 1 of the Hwang et al. reference discloses a circuit, which includes: a differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3), and complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground). Figure 1 of the Hwang et al. reference does not disclose that the flip-flop circuit includes another transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal receiving a clock signal. However, Figure 2 of the Choe reference discloses a flip-flop which includes a transistor (56) having a control terminal (gate) receiving a clock signal, a first current-handling terminal

connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of reducing power consumption and improving the speed of the circuitry (line 25 of Col. 2 to line 10 of Col. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the flip-flop circuit (Figure 1) of the Hwang et al. reference with a transistor connected between the outputs of the flip-flop circuit (i.e., a transistor connected between nodes Q and QN), as taught by the Choe reference (transistor 56 in Figure 2 of Choe), for the purpose of reducing power consumption and improving the speed of the circuitry. Thus, all of the limitations in claim 10 are met.

With respect to claim 11, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a first leg (12) including the first transistor (N3) and a second transistor (N4) connected in parallel, the second transistor (N4) having a second control terminal (gate) connected to the third input terminal (AN).

With respect to claim 12, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a second leg (12) having third and fourth transistors (N2, N1) connected in series, the third transistor (N2) having a third control signal (gate) connected to the second input terminal (B) and the fourth transistor (N1) having a fourth control terminal (gate) connected to the fourth input terminal (A).

11. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choe (USP 6,373,292) in view of Hwang et al. (USP 5,777,491), and further also in view of Choe (USP 6,373,292).

With respect to claim 15, Figure 2 of the Choe reference discloses a circuit (40) which includes an output stage (40), wherein the output stage (40) receiving a differential input signal (In, In/). Figure 2 of the Choe reference does not specially disclose how the differential input signal (In, In/) is generated. However, Figure 1 of the Hwang et al. reference discloses an input stage circuit that generate differential signal (Q, QN) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang et al. reference). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the circuit in Figure 1 of the Hwang et al. reference to provide the differential signal (Q, QN) to the differential input (In, In/) of the circuit in Figure 2 of the Choe reference (i.e., signals Q and QN in Figure 1 of the Hwang et al. reference are respectively to signals In and In/ in Figure 2 of the Choe et al. reference) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang et al. reference). Note that this combination meets all the limitation of this claim 15 except for the differential input stage (Figure 1 of the Hwang et al. reference) also includes another transistor having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal receiving a clock signal. However, Figure 2 of the Choe reference discloses a flip-flop which includes a transistor (56) having a control terminal (gate) receiving a clock signal, a first current-handling terminal connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of reducing power consumption and improving the speed of the circuitry (line 25 of Col. 2 to line 10 of Col. 3). It would have been obvious to one having

ordinary skill in the art at the time the invention was made to provide the differential input stage (Figure 1) of the Hwang et al. reference with a transistor connected between the outputs of the differential input stage as similar discussed in claim 10 above (i.e., a transistor connected between nodes Q and QN in Figure 1 of Hwang et al.), as taught by the Choe reference, for the purpose of reducing power consumption and improving the speed of the circuitry. Thus, this combination/modification meets all the limitation of claim 15, i.e., the above combination/modification includes an input stage (Figure 1 of the Hwang et al. reference) including a differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3), and complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground), and another transistor (as discussed in the modification discussed as similar to claim 10) having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal receiving a clock signal ; an output stage (Figure 2 of the Choe reference) including differential fifth and sixth input terminals (In and In/, Figure 2 of Choe) connected to respective ones of the first and second output terminals (Q and QN of Hwang et al.), complementary third and fourth output terminals (OUT and OUT/ in Figure 2 of Choe), and a transistor (56, Figure 2 . of Choe) having a control terminal (gate), a first current-handling terminal (64, Figure 2 of Choe) connected to the third output terminal (OUT, Figure 2 of Choe) and a second current-handling

terminal (62, Figure 2 of Choe) connected to the fourth output terminal (OUT/, Figure 2 of Choe).

With respect to claim 16, Figure 2 of the Choe reference in the above combination also meets the limitation of a clock terminal (CLK/) connected to the control terminal (gate of transistor 56 in Figure 2 of Choe).

Allowable Subject Matter

12. Claims 17-20 are allowed.

Claim 17 is allowed because the prior art of record does not disclose or suggest a counter circuit which includes a first and second flip-flops in which the first flip-flop including a cross coupled transistor directly connected to a positive power supply voltage and a first transistor, and the second flip-flop including a second transistor connected to the third input terminal and a current handling terminal directly connected to Vss and a third transistor with the recited connections set forth therein.

Claims 18-20 are allowed because they depend on claim 17.

Response to Arguments

13. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection as discussed above.

Note that applicant also argues that "Claim 10 is not obvious under 25 U.S.C. 103(a) in view of Hwang combined with Choe. Choe in FIG. 2 has a transistor 56 coupled between output terminals 58 and 60, but does not have a transistor with a control terminal connected to an input terminal and a current handling terminal directly connected to VSS. The current handling terminal in Choe is connected via transistor 52 to ground. Transistors 56 and 52 work in concert

and are alternatively on and off depending on the clock and its complement. The removal of transistor 52 in Choe in order to combine Choe with Hwang would change the principle of operation of the circuit of Choe and hence the reference cannot be combined".

In response to applicant's argument that the claim is not obvious, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, the primary reference (Figure 1 of Hwang) meets all the limitations of the claim except for a transistor connected between the output terminals of the differential stage, and the secondary reference (Figure 2 of Choe) teaches that a transistor (56) is connected between the output terminals of a differential stage provides advantages such as of reducing power consumption and improving the speed of the circuitry, and therefore it is obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Hwang reference by providing a transistor connected between the output terminals Q and QN for the purpose of reducing power consumption and improving the speed of the circuitry. Therefore, the 103 rejection is proper.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: July 25, 2003

Long Nguyen
Art Unit: 2816